Fig. 1A (Prior Art)

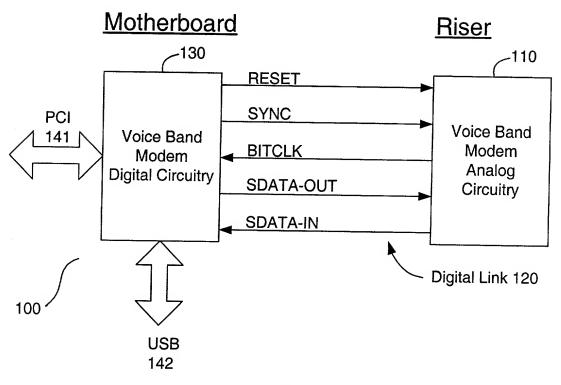
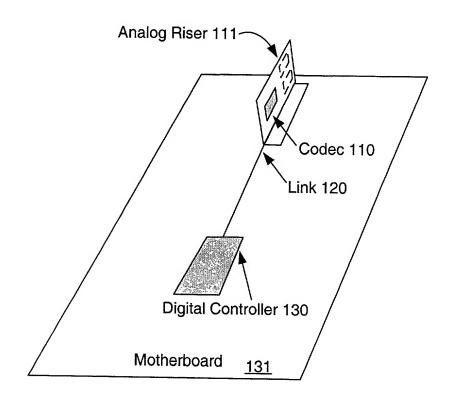
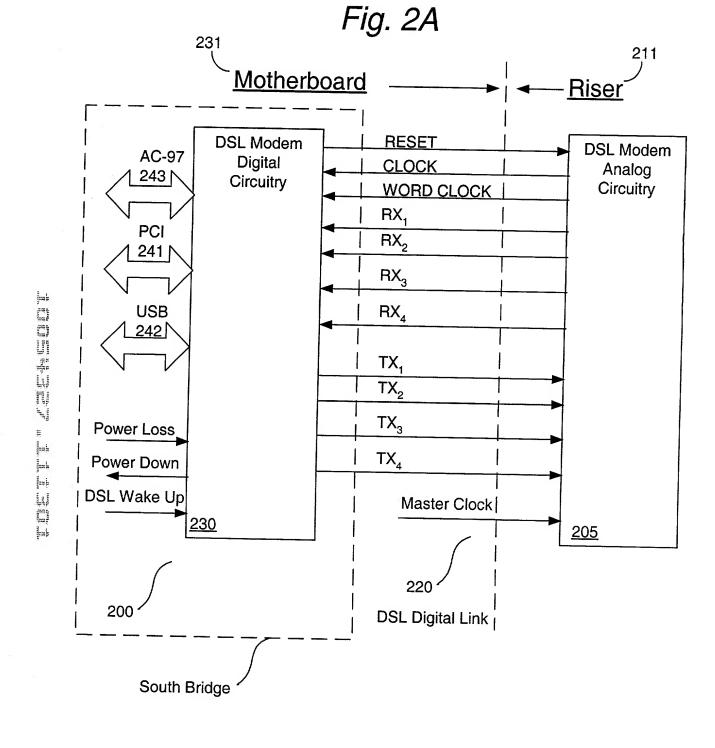
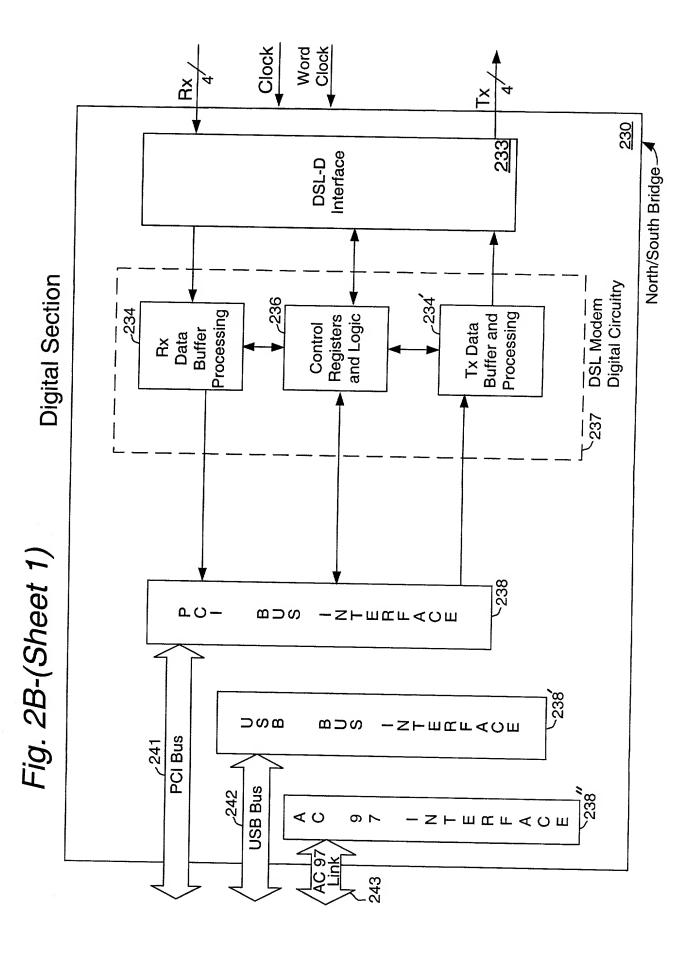
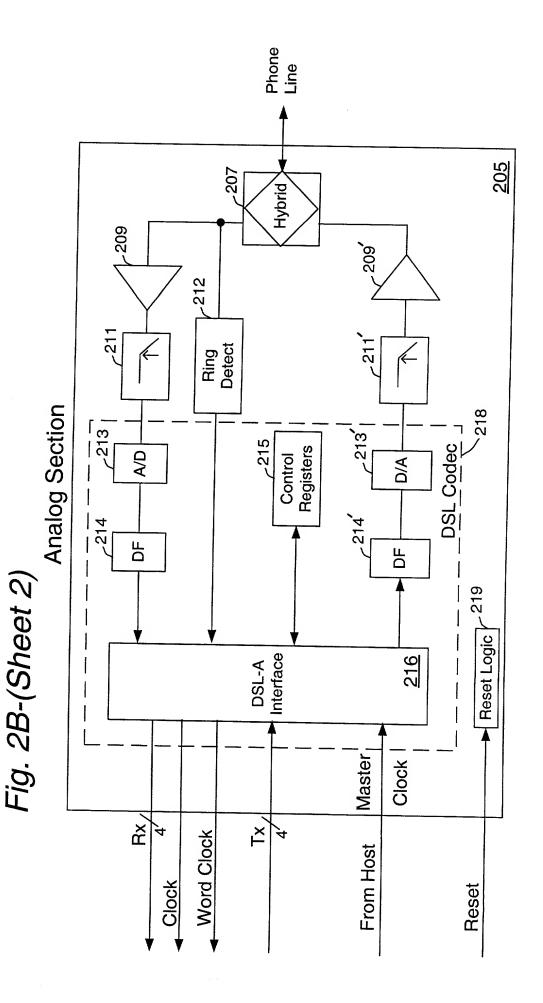


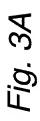
Fig. 1B











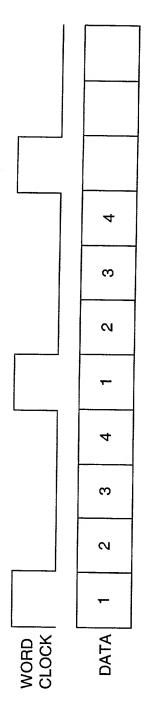


Fig. 3B

	0	6	_ >		
	8	g	_		
	5		B1		
	D2		B2		
	D3		B3		
	, D6 D5 D4		84		
			B5		
			B6		
	D2		B7		
	D9 D8		B8		
			B10 B9		
	D10		B10		
	D11		B11		
	D15 D14 D13 D12 D11 D10 D9		B12		
			B13		
			B14 B13 B12		
			S C C		

Fig. 3C

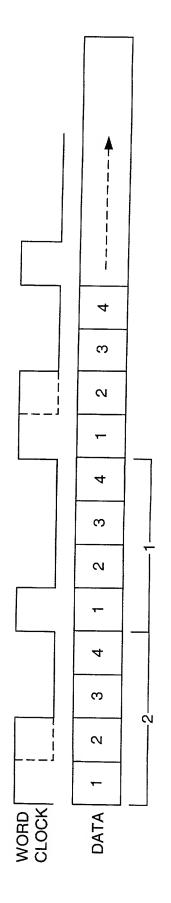


Fig. 4

			7		1	
	Cycle 4		RxData[3:0]		TxData[3:0]	
	Cycle 2 Cycle 3		RxData[7:4]		TxData[7:4]	
			RxSOC, RxAddr.[2:0]		TxSOC,TxAddr.[2:0]	
	Cycle 1		Control, 0, RxClav, TxClav		Control, 0, RxEnb, TxEnb	
	DSL Link Pins		RxData[3:0] TxData[3:0]		TxData[3:0]	